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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
HENRY, MATTHEW ALLAN	
ART UNIT	**PAPER NUMBER**
2116	

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Please find below and/or attached an Office communication concerning this application or proceeding.

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Office Action Summary	Application No. 10/032,942	Applicant(s) BRESNIKER ET AL.
	Examiner Matthew A. Henry	Art Unit 2116

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4,5,7 and 8* is/are rejected.

7)☒ Claim(s) *3,6 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 December 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dempsey (6,418,540) in view of Cramer (6,728,897).

Regarding Claim 1, to provide fault tolerance in a multiprocessor device with power conservation in mind (Column 2, Lines 25-30), Dempsey teaches:

"A method of providing minimal power consuming redundant computing elements" (Column 2, Lines 25-31),

A "plurality of computing elements (Figure 1, Items 117, 157) that can each enter a power saving mode" (Column 1, Lines 36-38 and Column 7, Line 2).

"detecting an impending or actual failure of an affected computing element" (Column 1, Lines 25-35. While the disclosure does not expressly discuss a detection method, it discloses an interrupt that initiates the transition from an active to a spare processor. The detection of failure must necessarily precede the generation of this interrupt, therefore detecting an impending or actual failure is an inherent characteristic of the Dempsey device.);

"signaling a cold spare computing element to enter a normal operation mode from the power saving mode" (Column 3, Lines 57-61);

"initializing instances of identified components on the cold spare computing element now operating in normal operation mode" (Column 6, Lines 23-27).

Dempsey does not address the identification of application components or the initialization thereof.

Focusing on persistence of applications and data in a fault tolerant multiprocessor device (Column 2, Lines 25-29), Cramer teaches:

"a distributed application comprised of a plurality of components" (Column 2, Lines 32-35),

"identifying instances of components executing on the affected computing element" (Column 4, Lines 12-14. The processor identifies what it is running by indicating what it cannot do.);

"initializing instances of identified components (Column 4, Lines 40-41) on the cold spare computing element now operating in normal operation mode."

While Cramer does not consider running redundant processors in a low power mode, he does further maximize the potential of these extra components by enabling these processors to identify and receive the data and processes running on a failing processor (Column 2, Lines 29-30).

Dempsey and Cramer both define ways to efficiently use secondary, functional processors to supplant a failing one, but they achieve this goal in different methods. It would have been obvious to a person of ordinary skill in the art to apply combine the power saving hardware redundancy scheme detailed in Dempsey with the ability to sustain active applications by transferring them from a failing processor to a functioning one as described in Cramer.

The motivation for doing so would be to give power efficient redundant hardware systems the capacity to sustain running applications to, as explained by Cramer, "maintain high availability of information and use available resources to their maximum potential" (Column 2, Lines 29-30).

Regarding Claim 4, to provide fault tolerance in a multiprocessor device with power conservation in mind (Column 2, Lines 25-30), Dempsey teaches:

"A computer program product comprising:
at least one computer usable medium having computer readable code embodied therein," (Column 7, Lines 19-22).

"for providing availability of minimal power consuming redundant computing elements," (Column 2, Lines 25-31).

"a plurality of computing elements (Figure 1, Items 117, 157) that can each enter a power saving mode," (Column 1, Lines 36-38 and Column 7, Line 2).

"first computer readable program code devices configured to detect an impending or actual failure of an affected computing element," (Column 1, Lines 25-35. While the disclosure does not expressly discuss a detection method, it discloses an interrupt that initiates the transition from an active to a spare processor. The detection of failure must necessarily precede the generation of this interrupt, therefore detecting an impending or actual failure is an inherent characteristic if the Dempsey device.).

"third computer readable program code devices configured to signal a cold spare computing element to enter a normal operation mode from the power saving mode," (Column 6, Lines 23-27).

Dempsey does not discuss the identification of application components or the initialization thereof.

Focusing on persistence of data in a fault tolerant multiprocessor device (Column 2, Lines 25-29), Cramer teaches:

"a distributed application comprised of a plurality of components, (Column 2, Lines 32-35).

"second computer readable program code devices configured to identify instances of components executing on the affected computing element," (Column 4, Lines 12-14. The processor identifies what it is running by indicating what it cannot do.).

"fourth computer readable program code devices configured to initialize instances of identified components (Column 4, Lines 40-41) on the cold spare computing element now operating in the normal operation mode."

The motivation behind Cramer's invention has already been discussed in paragraph 8 above.

Dempsey and Cramer both define ways to efficiently use secondary, functional processors to supplant a failing one, but they achieve this goal in different methods. It would have been obvious to a person of ordinary skill in the art to apply combine the power saving hardware redundancy scheme detailed in Dempsey with the ability to sustain active applications by transferring them from a failing processor to a functioning one as described in Cramer.

The motivation for doing so would be to give power efficient redundant hardware systems the capacity to sustain running applications to "maintain high availability of information and use available resources to their maximum potential" (Column 1, Lines 7-11).

Regarding Claim 7, to provide fault tolerance in a multiprocessor device with power conservation in mind (Column 2, Lines 25-30), Dempsey teaches:

"a backplane," (Column 3, Line 66).

"a plurality of host processor cards coupled to the backplane," (Column 3, Lines 39-40).

"at least one of the plurality of cards designated as a cold spare host processor card that is normally kept in a power saving mode," (Column 1, Lines 36-38 and Column 7, Line 2).

"a management unit coupled to the back plane," (Column 3, Lines 39-40 and 57-6; While the disclosure does not expressly discuss a management unit, it discloses an interrupt that initiates a transition from an active processor to a spare processor including the switching of these processors into a sleep and active state. The creation of this interrupt must necessarily originate from a location tied to this communication bus, therefore a management unit coupled to the back plane is an inherent aspect of the Dempsey device.)

"the management unit operable to signal each of the plurality of host processor cards to enter the power saving mode and a normal operation mode (Column 3, Lines 57-61. Again, the disclosure does not expressly discuss a management unit capable of signaling to processors to transition to power saving or normal operation modes. However, it does disclose an interrupt capable of enacting such changes. The generation of this interrupt must necessarily originate from a location capable of enabling this signal, therefore a management unit operable to signal

each of the plurality of host processor cards to enter the power saving mode and a normal operation mode is an inherent aspect of the Dempsey device.).

"detects an impending or actual failure of an affected host processor card of the plurality of host processor cards," (Column 1, Lines 25-35. While the disclosure does not expressly discuss a detection method, it discloses an interrupt that initiates the transition from an active to a spare processor. The detection of failure must necessarily precede the generation of this interrupt, therefore detecting an impending or actual failure is an inherent characteristic if the Dempsey device.).

"signals the cold spare host processor card to enter the normal operation mode from the power saving mode," (Column 6, Lines 23-27).

Dempsey does not discuss the identification of application components or the initialization thereof.

Focusing on persistence of data in a fault tolerant multiprocessor device (Column 2, Lines 25-29), Cramer teaches:

"a distributed application comprised of a plurality of components," (Column 2, Lines 32-35).

"executing a program that identifies instances of components executing on the affected host processor card," (Column 4, Lines 12-14. The processor identifies what it is running by indicating what it cannot do.).

"executing a program that initializes instances of identified components (Column 4, Lines 40-41) on the cold spare host processor card now operating in normal operation mode."

The motivation behind Cramer's invention has already been discussed in paragraph 8 above.

Dempsey and Cramer both define ways to efficiently use secondary, functional processors to supplant a failing one, but they achieve this goal in different methods. It would have been obvious to a person of ordinary skill in the art to apply combine the power saving hardware redundancy scheme detailed in Dempsey with the ability to sustain active applications by transferring them from a failing processor to a functioning one as described in Cramer.

The motivation for doing so would be to give power efficient redundant hardware systems the capacity to sustain running applications to "maintain high availability of information and use available resources to their maximum potential" (Column 1, Lines 7-11).

3. Claims 2, 5 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dempsey in view of Cramer as applied to claims 1, 4 and 7 above, and further in view of Lanus (6,161,197).

Regarding Claim 2, Cramer further teaches:

"Gracefully suspending all instances of identified components, if possible, executing on the affected computing element," (Column 4, Lines 28-31).

Cramer does not discuss signaling an affected computing element to enter a hot swap mode.

To allow for a failed processor in a multiprocessor system to be "corrected without interrupting operation of the system," (Column 5, Line 41) Lanus teaches:

"Signaling the affected computing element to enter a hot swap mode from the

normal operation mode," (Column 7, Lines 37-40).

Lanus' motivations for providing a fault tolerant multiprocessing system with this capability is that it allows for faulty components in a fault tolerant multiprocessor system to be repaired or replaced "without interrupting operation of the system" (Column 5, Lines 39-41).

Dempsey, Cramer and Lanus are all intent on modifying existing fault tolerant multiprocessing systems to be more efficient when a failure does occur, but all have found different ways of meeting that end. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the ability to render a failed processor "hot swappable" as described by Lanus in Column 7, Lines 37-40 with the invention deemed obvious by Dempsey and Cramer in paragraph 6 above.

The motivation for doing so would have been to create a fault tolerant system that can "withstand a system host failure without interrupting operation of the system" as described by Lanus in Column 1, Lines 49-50 and result in a "fully functional cluster and the best possible information availability while being executed as described by Cramer in Column 2, Lines 22-24.

Regarding Claim 5, Cramer further teaches:

"Fifth computer readable program code devices configured to gracefully suspend all instances of identified components, if possible, executing on the affected computing element," (Column 4, Lines 28-31).

Cramer does not discuss signaling an affected computing element to enter a hot swap mode.

To allow for a failed processor in a multiprocessor system to be "corrected without interrupting operation of the system," (Column 5, Line 41) Lanus teaches:

"Sixth computer readable program code devices configured to signal the affected computing element to enter a hot swap mode from the normal operation mode," (Column 7, Lines 37-40).

The motivation behind Cramer's invention has already been discussed in paragraph 11 above.

Dempsey, Cramer and Lanus are all intent on modifying existing fault tolerant multiprocessing systems to be more efficient when a failure does occur, but all have found different ways of meeting that end. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the ability to render a failed processor "hot swappable" as described by Lanus in Column 7, Lines 37-40 with the invention deemed obvious by Dempsey and Cramer in paragraph 6 above.

The motivation for doing so would have been to create a fault tolerant system that can "withstand a system host failure without interrupting operation of the system" as described by Lanus in Column 1, Lines 49-50 and result in a "fully functional cluster and the best possible information availability while being executed as described by Cramer in Column 2, Lines 22-24.

Regarding Claim 8, Cramer further teaches:

"The program executing on the management unit also:

gracefully suspends all instances of identified components, if possible, executing on the affected host processor card," (Column 4, Lines 28-31).

Cramer does not discuss the management signaling an affected computing element to enter a hot swap mode.

To allow for a failed processor in a multiprocessor system to be "corrected without interrupting operation of the system," (Column 5, Line 41) Lanus teaches:

"the program executing on the management unit also:

> signals the affected host processor card to enter a hot swap mode from the normal operation mode," (Column 7, Lines 37-40).

The motivation behind Cramer's invention has already been discussed in paragraph 11 above.

Dempsey, Cramer and Lanus are all intent on modifying existing fault tolerant multiprocessing systems to be more efficient when a failure does occur, but all have found different ways of meeting that end. At the time of the invention it would have been obvious to a person of ordinary skill in the art to incorporate the ability to render a failed processor "hot swappable" as described by Lanus in Column 7, Lines 37-40 with the invention deemed obvious by Dempsey and Cramer in paragraph 6 above.

The motivation for doing so would have been to create a fault tolerant system that can "withstand a system host failure without interrupting operation of the system" as described by Lanus in Column 1, Lines 49-50 and result in a "fully functional cluster and the best possible information availability while being executed as described by Cramer in Column 2, Lines 22-24.

Allowable Subject Matter

4. Claims 3, 6 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Slegel discloses a multiple processor computer that implements at least one spare processor that is "simply waiting to be 'awakened' if it is needed to take over from a failed processor" (Column 3, Lines 26-29).

Lomet discloses a method for identifying multiple, running applications by implementing a table that includes an application ID field (Column 10, Lines 16-21). The table is used for purposes of recovering an application's state prior to a crash (Column 9, Lines 37-39).

Response to Arguments

6. Applicant's arguments filed on December 6, 2004 have been fully considered but they are not persuasive.

Regarding Claims 1, 4 and 7, the Applicant states that he:

"does not understand Cramer to teach or address the initialization of applications components, since the components are already operational and initialized" (Page 14, Paragraph 4, Lines 10-12).

Cramer states, "the second filer 120 assumes the tasks of the first filer 110 through a takeover process" (Column 4, Lines 40-41). There is no evidence in Cramer to suggest that these processes are already operational and initialized. For the tasks previously running on the first filer to be successfully taken over for processing by the second filer, the tasks must be initiated on the second filer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew A. Henry whose telephone number is (571) 272-3845. The examiner can normally be reached on Monday - Friday (8:00 am -5:00 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MAH

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